entitled "Process for Reducing the Critical Dimensions of Integrated Circuit Device Features;" U.S. Application No. 09/819,342 (Atty. Dkt. No. 39153/403) by Shields et al., entitled "Process for Forming Sub-Lithographic Photoresist Features by Modification of the Photoresist Surface;" and U.S. Application No. 09/819,552 (Atty. Dkt. No. 39153/310) by Gabriel et al., entitled "Process for Improving the Etch Stability of Ultra-Thin Photoresist," all filed on an even date herewith and assigned to the Assignee of the present application.

In the Claims:

In accordance with 37 CFR § 1.121, please substitute for original claims 9, 13, 14 and 19 the following rewritten versions of the same claims, as amended. The changes are shown explicitly in the attached "Marked Up Version Showing Changes Made."

Please amend the following claims 9, 13, 14 and 19.

9. (Amended) An integrated circuit fabrication process, the process comprising:

developing a patterned photoresist layer, the patterned photoresist layer including at least one feature;

modifying the patterned photoresist layer to form a top portion and a bottom portion of the at least one feature, the top portion having a top etch rate and the bottom portion having a bottom etch rate, wherein the top etch rate is different from the bottom etch rate; and

trimming the patterned photoresist layer to change the at least one feature to have a sub-lithographic lateral dimension, whereby a sufficient vertical thickness exists to maintain pattern integrity, wherein the modifying step is performed after the developing step and before the trimming step.

13. (Amended) The process of claim 12, wherein a majority of the top portion and a laterally trimmed bottom portion comprises the at least one feature upon completion of the modifying step, the laterally trimmed bottom portion having the sub-

lithographic lateral dimension and the sufficient vertical thickness to maintain pattern integrity.

14. (Amended) The process of claim 13, further comprising removing the majority of the top portion after the modifying step to form a trimmed feature.

19. (Amended) The process of claim 18, wherein the top portion has an etch rate 15-70% slower than an untreated etch rate of the photoresist layer during the trimming step.